

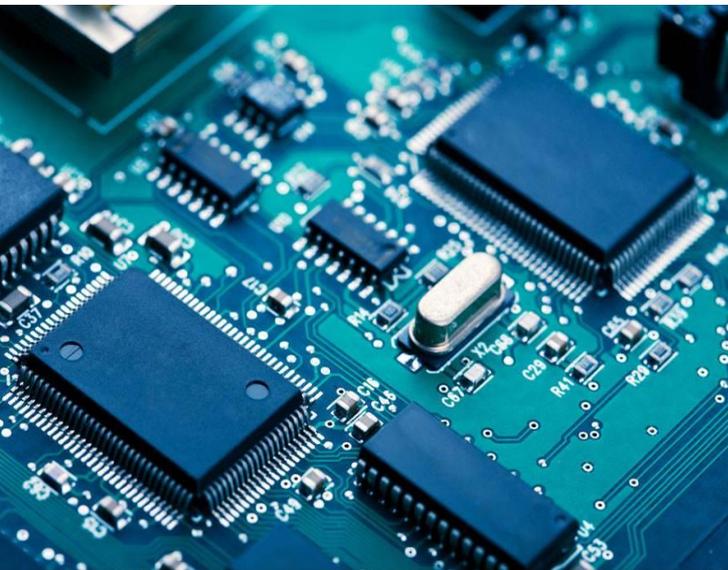


SILINTECH

苏州芯联成软件有限公司

[www.silintech.com](http://www.silintech.com)

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# 公司介绍



芯联成科技有限公司(Silintech)成立于2015年, 主要从事芯片工艺分析, EDA软件研发和电路竞争力分析等业务。2016年, 在苏州建有专业芯片分析实验室, 拥有多台SEM, ICP, RIBE等高阶分析设备, 能为客户提供成熟的14nm以上芯片工艺分析技术服务。公司自主研发的EDA软件Bunny, 能为客户提供更完整、快速、先进与创新之高质量电路分析技术服务, 与全球领先趋势共同成长。

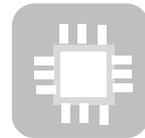
日新月异的工艺/电路, 越来越小的工艺节点, TSV, FinFET, MEMS, BSI, CIS, PV, LED, Advance Memory等新工艺, 存在大量技术创新, 芯联成将助力电子工程师深入探索。



拥有专业的芯片分析实验室, 通过先进的芯片解剖技术, 能处理28~10nm的高阶工艺制程芯片去层



自主研发的EDA软件, 包括IC芯片图像采集系统和IC电路分析系统



深度解析市场成熟产品, 帮助客户攻克核心技术难题, 减少市场进入壁垒, 实现更好的产品兼容度



通过成本分析了解新产品的研发成本, 降低研发风险

# 公司介绍



在北京、银川、芜湖、台湾分设电路提取、电路整理、业务部。团队总人数达200多人。公司运营总部设在苏州，构建有完整的人力资源、财务、销售、以及软件研发和电路分析等部门。



## Laboratory

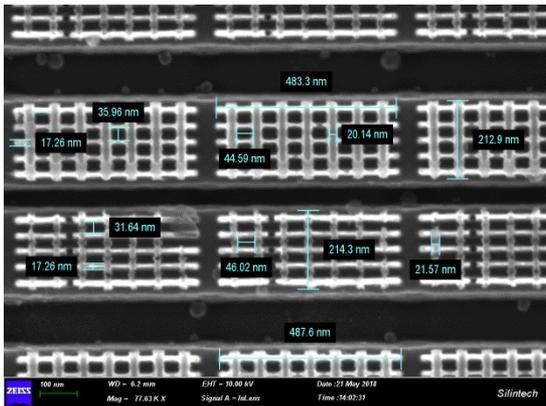
RIE/IBE刻蚀

SEM/OM显微图像采集

CMP化学机械研磨



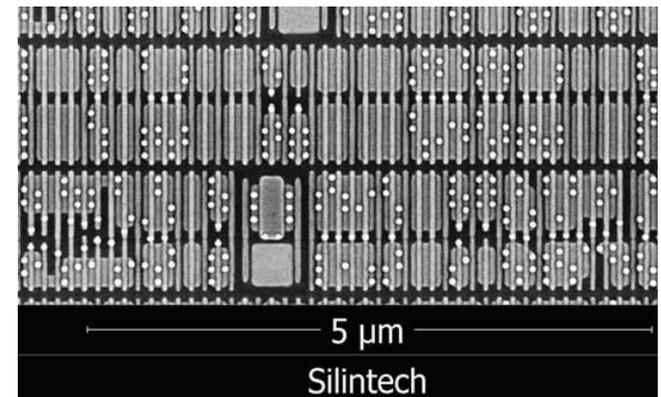
- 可以剖析28nm/14nm等高阶工艺制程的芯片，也可以对7~10nm工艺的芯片作局部剖析。以刻蚀方式去除，包括去除保护层、氧化层、钝化层、金属层等。
- 各种芯片染色技术：Single Well染色、Deep Well染色和ROM码点染色。
- Al、Au、Cu等各种工艺芯片的解剖。
- BCD、SOI、GaAs、SiGe、BiCMOS、GaN等多种特殊工艺芯片剖析。



14nm FinFET



10nm M1



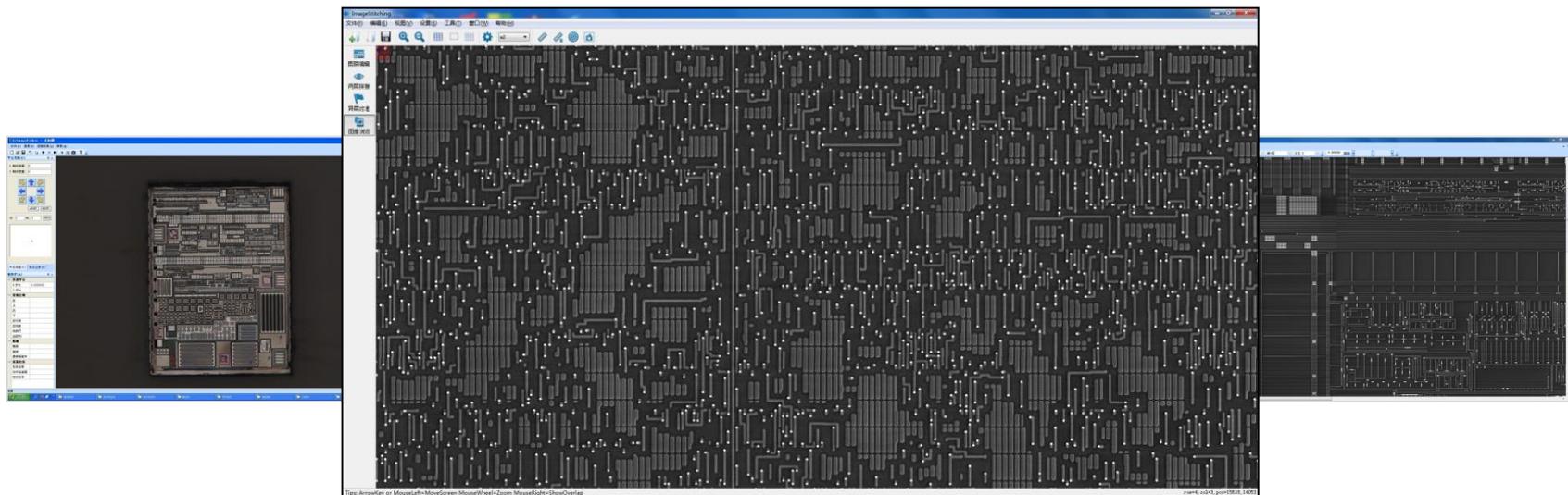
28nm Poly

## IC芯片图像采集系统

ICImagePicker 光学影像采集软件

SemPicker 扫描电子显微图像采集软件

ImageStitching 自动拼图软件



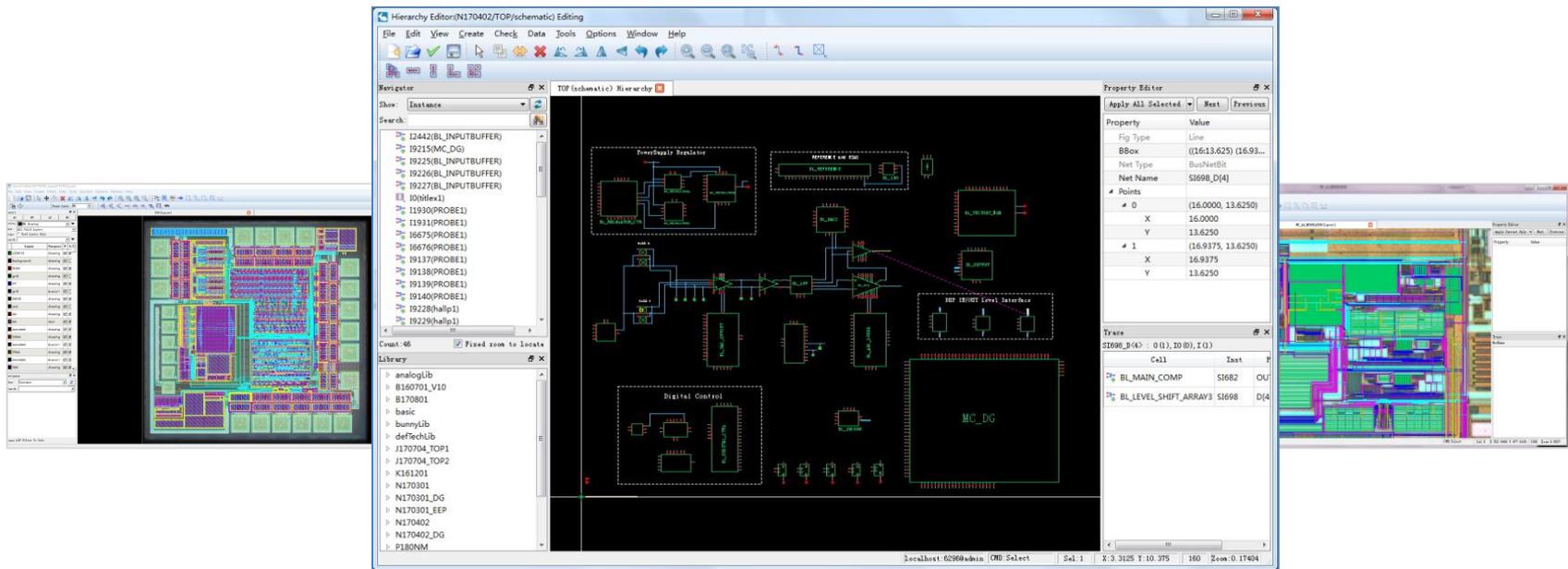
良好的人机交互，一键采集  
量化移动图像，精准移动图像  
自动计算行列数，获取采集张数  
自动聚焦拍照，无需人工干预完成采集

专业友好的人机交互界面  
支持数百G的图像容量  
拼接误差：半个孔以内  
支持JPG、GIF、PNG等常用图像格式

自动曝光及白平衡，快速对焦  
支持同层自动拼接，自动纠偏  
支持整图导出及区域导出  
支持图像的旋转、缩放及多窗口显示

## IC电路分析系统

电路版图编辑和电路标注软件  
原理图编辑和电路整理软件



海量IC照片均可在0.1秒内显示  
线网自动识别、单元自动搜索  
支持实时DRC, 提供相应错误报告

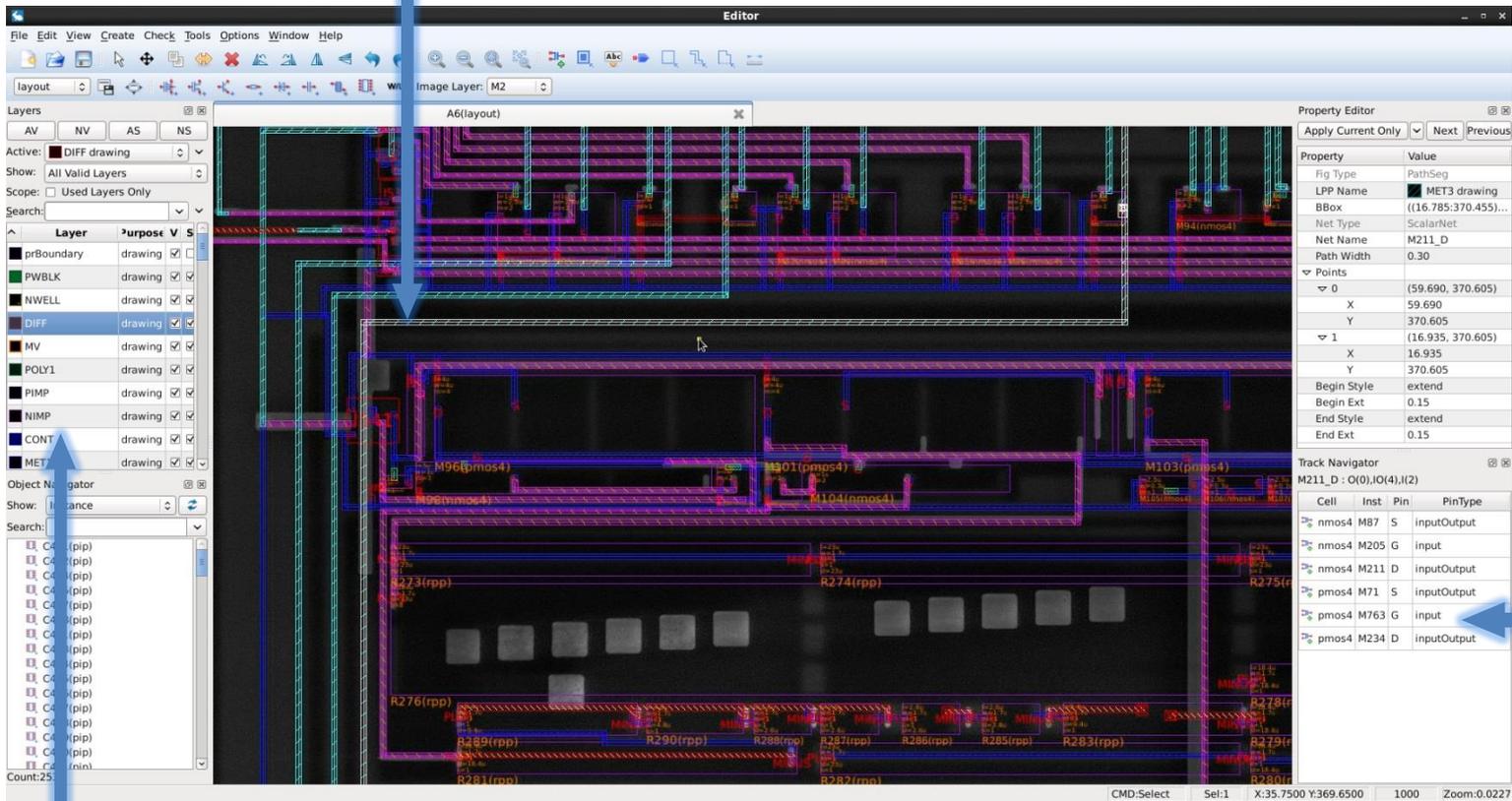
数据兼容主流EDA设计软件  
支持百万门级电路的分析

支持多用户协同工作  
具有层次化线网追踪功能

- ✓ 自主研发的EDA软件Bunny，其内核基于SI2组织发布的OpenAccess数据库，可以与**各大主流EDA设计软件（Cadence, Synopsys, Mentor）完全兼容**，无需数据导入导出。也支持导出为CDB、EDIF200、SPICE、Verilog格式，以便其他软件调用和仿真验证。
- ✓ 引入**AI算法**，大幅度**提高**了大规模数字电路提取的**识别效率**和**准确率**。
- ✓ 自主研发的**电路同构和相似搜索算法**，大幅度**提高**了电路**分析整理效率**。
- ✓ 可进行**百万门级**数字电路的自动提取分析。
- ✓ 可**多人并行操作**，多人合作编辑同一个单元。提供**单元、线网自动跟踪，自动维护连接关系的一致性**，方便电路的浏览和整理。
- ✓ 芯片**照片加密**打包提高了**数据安全性**，支持**TB级海量照片的快速浏览**。
- ✓ 采用C/S网络模式，服务器和客户端**可跨平台运行，支持异地远程操作**。

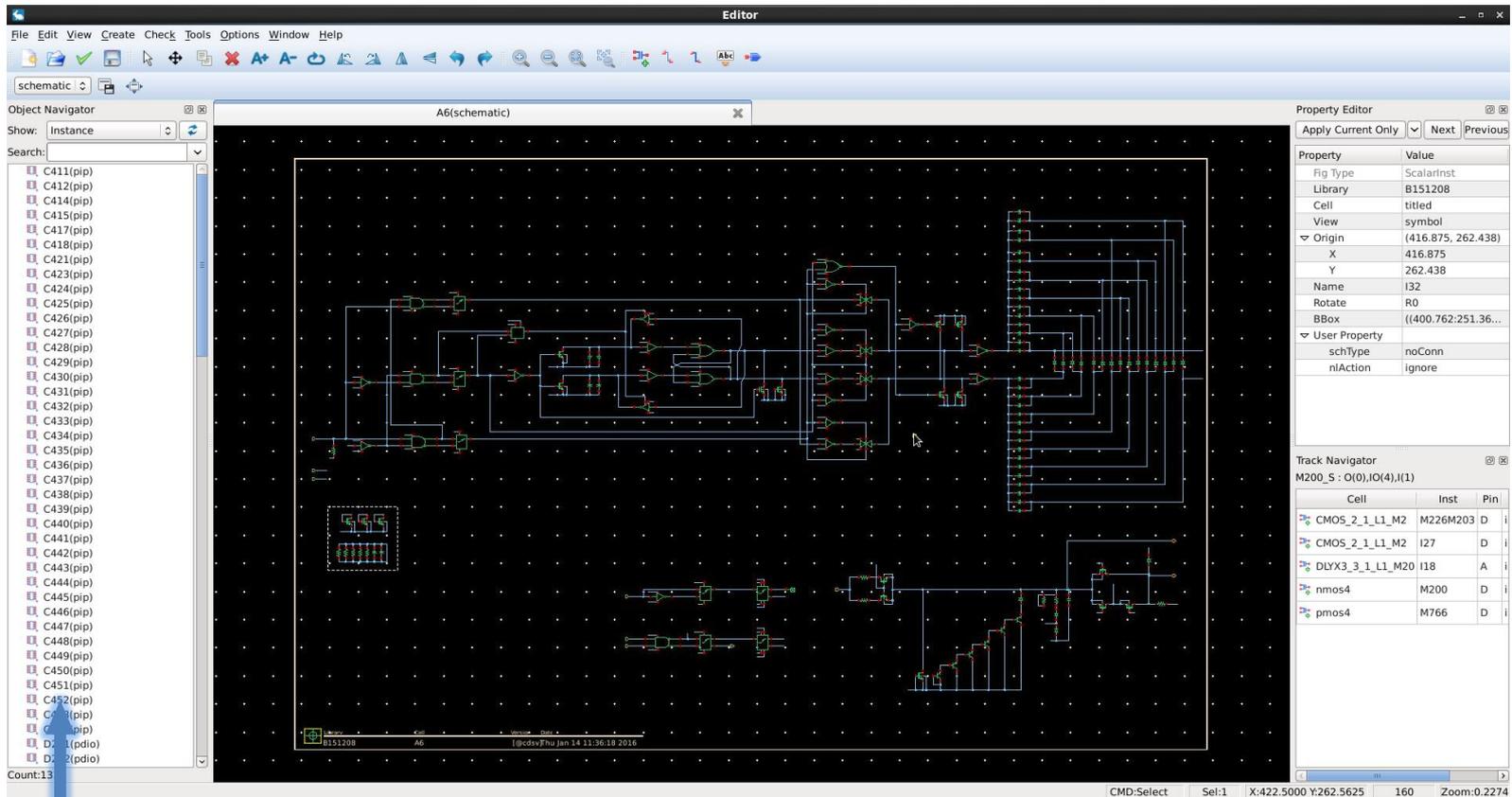
## Layout / Annotate View

Double click path to show connection information



Full function layout editor

## Schematic / Hierarchy View



Object Navigator for component quick positioning

1

Sector

## 芯片工艺分析

芯片开盖、芯片取晶粒、去层解剖、芯片染色、光学和电子显微拍照、失效分析等。

2

Sector

## 电路竞争力分析

网表提取、版图设计、电路整理、逻辑和电路仿真和芯片解密等。

3

Sector

## 专利侵权分析

专利侵权规避、专利无效抗辩、布图设计独创性鉴定、商业秘密侵权分析和专利地图等。

4

Sector

## 芯片设计分析

停产芯片/军用芯片仿制、后端设计、芯片设计等。

5

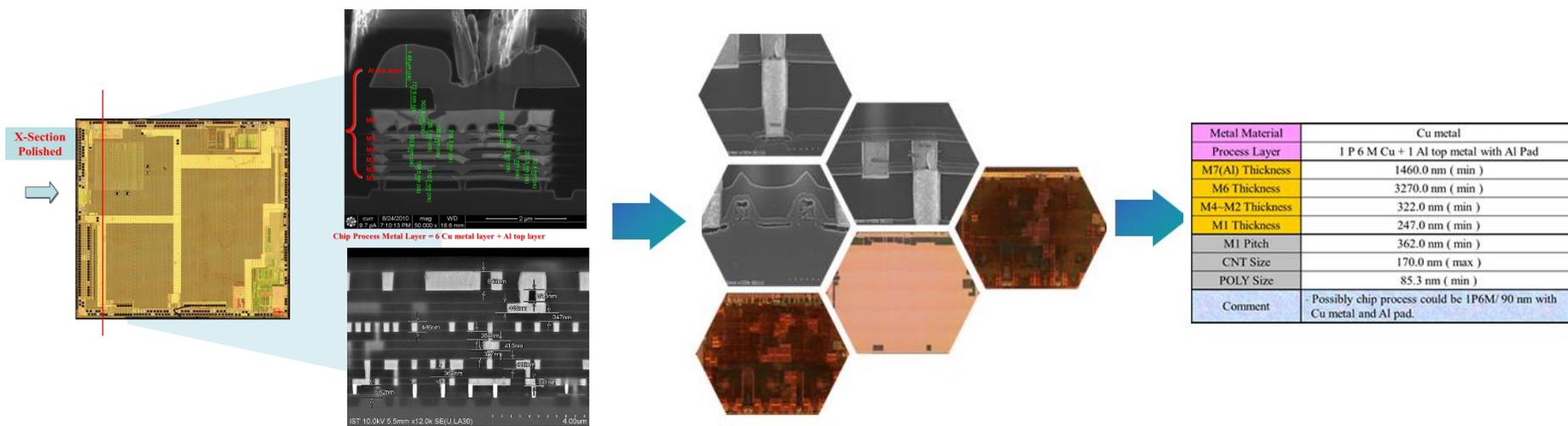
Sector

## 第三方代理服务

流片、封装和测试等服务。

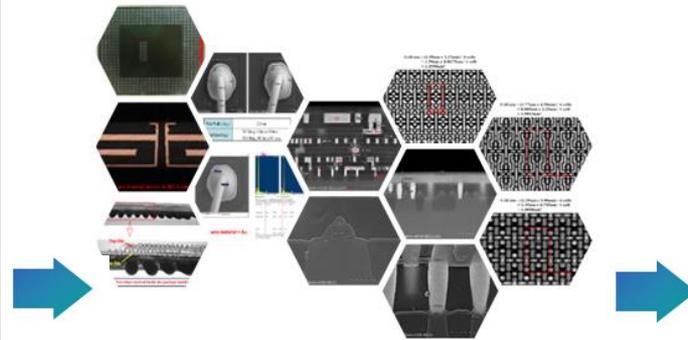
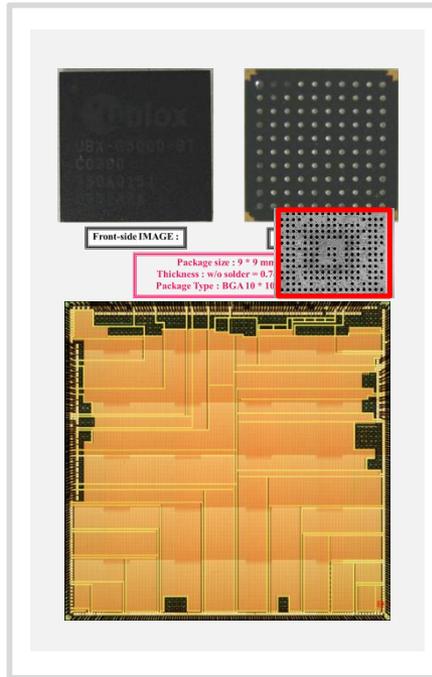


通过**芯片工艺制程分析**，取得领先的工艺器件结构设计原理，帮助后端工艺工程师快速成长。

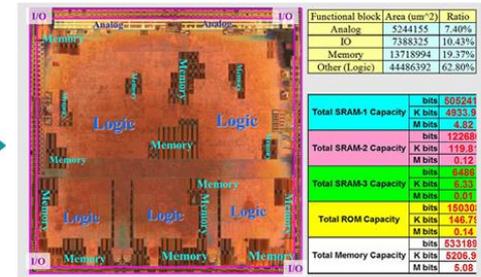


## 工艺制程分析

**成本分析**，即在材料分析的基础上，通过对芯片结构与成分的逐层分析，为客户提供最经济的产品设计或生产方案。

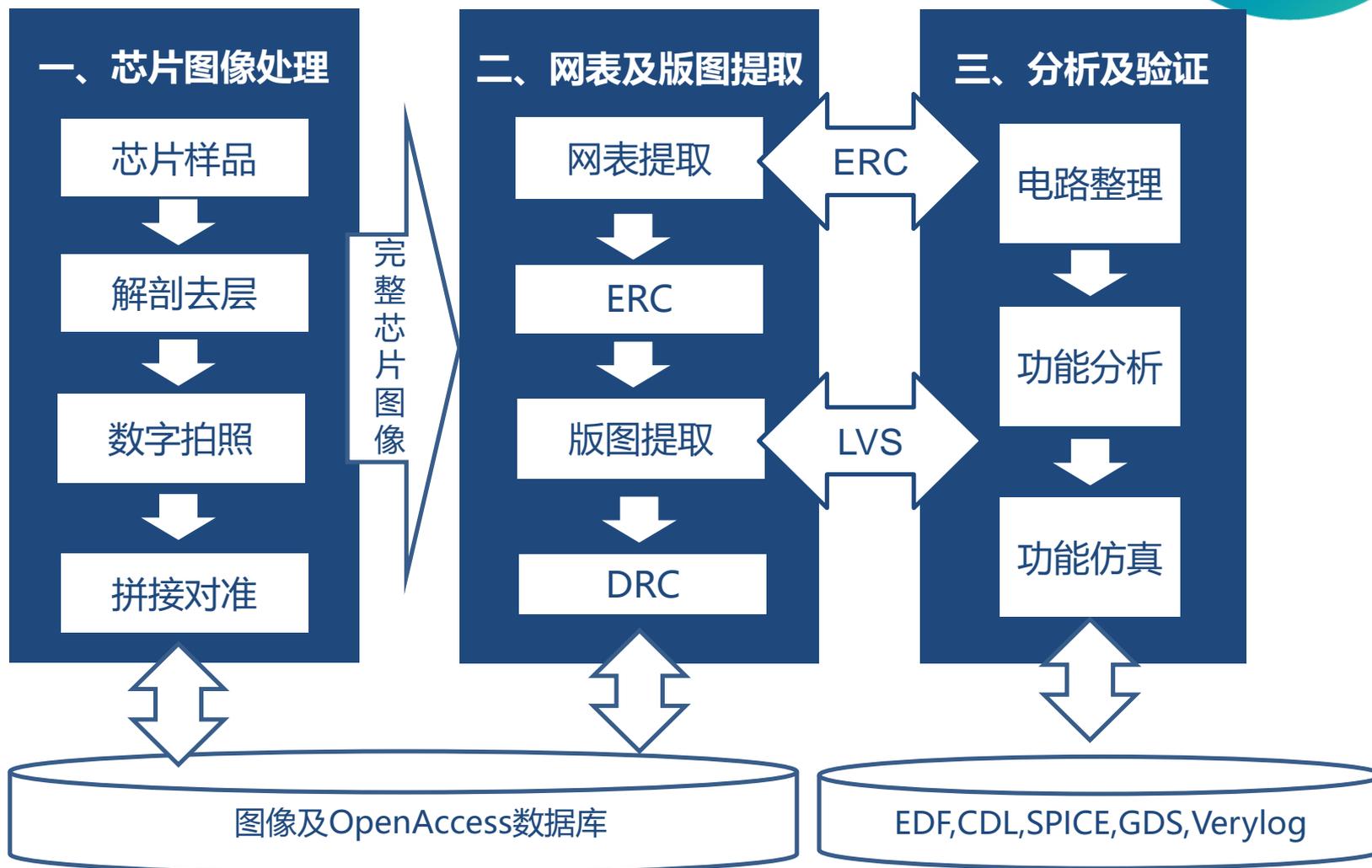


Metal Material	Cu metal
Process Layer	1P7M Cu metal + Al top layer
M1 Thickness	263 nm ( min )
M1 Pitch	269 nm ( min )
CNT Size	147 nm ( max )
POLY Size	88.5 nm ( min )
Comment	- Possibly chip process could be 1P6M/ 90nm with Cu process and Al top layer.



## 成本分析

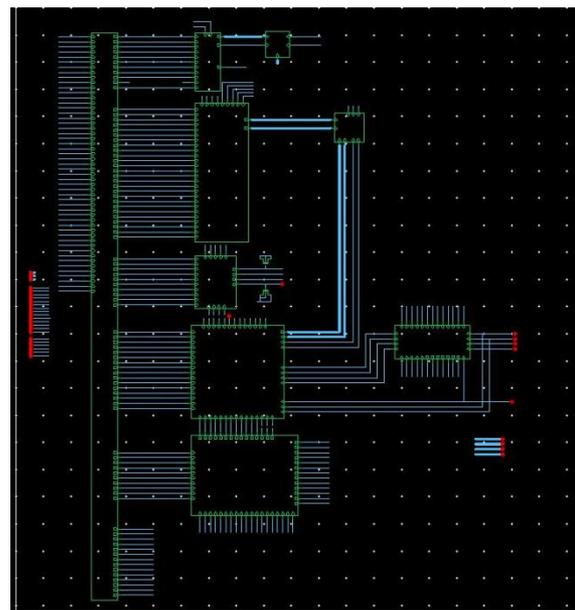
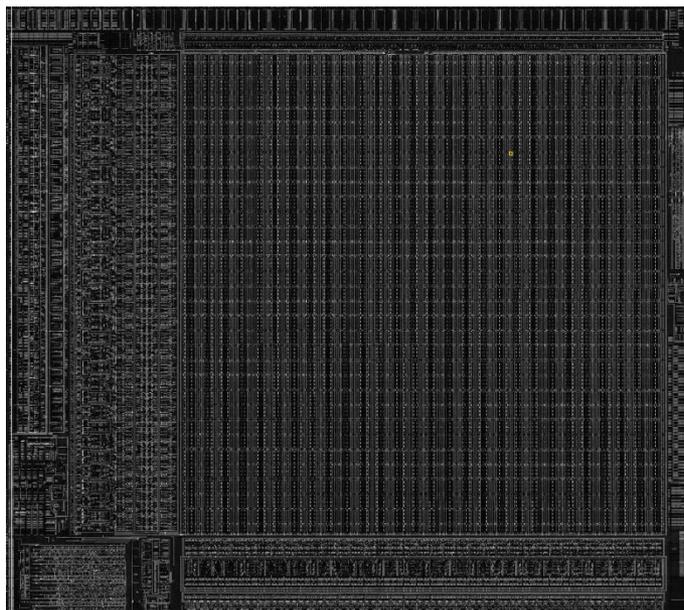
## 集成电路竞争力分析流程图



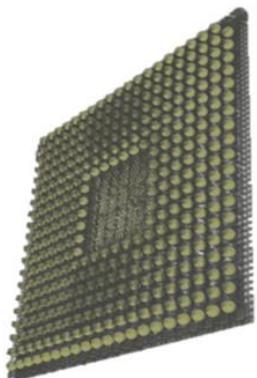


## ■ EEPROM/Flash数据分析

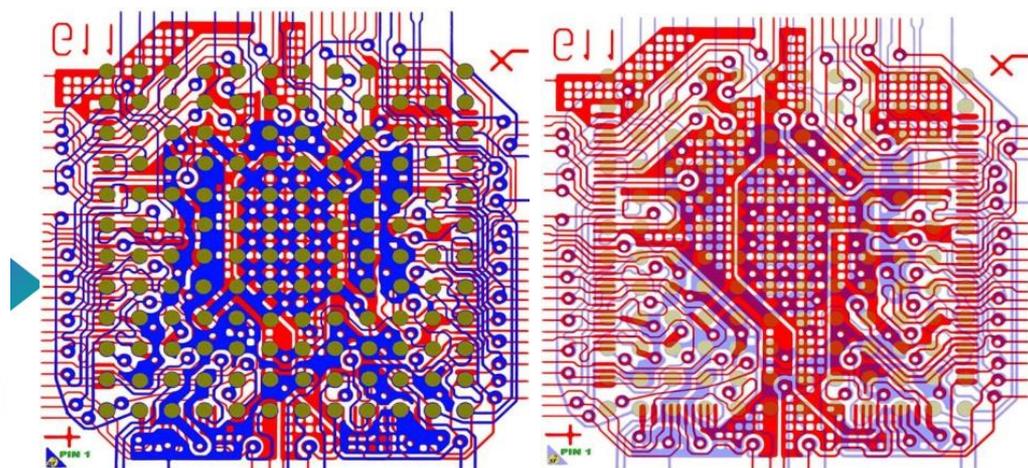
通过对EEPROM/Flash译码等电路的分析，找到关键电路或加密电路，并利用FIB的电路修改功能屏蔽加密电路，即可读取EEPROM/Flash中的程序。



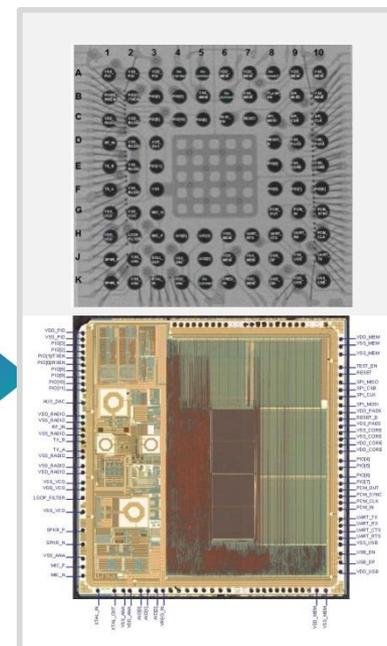
## ■BGA封装分析 (PIN To Ball)



3DX -Ray

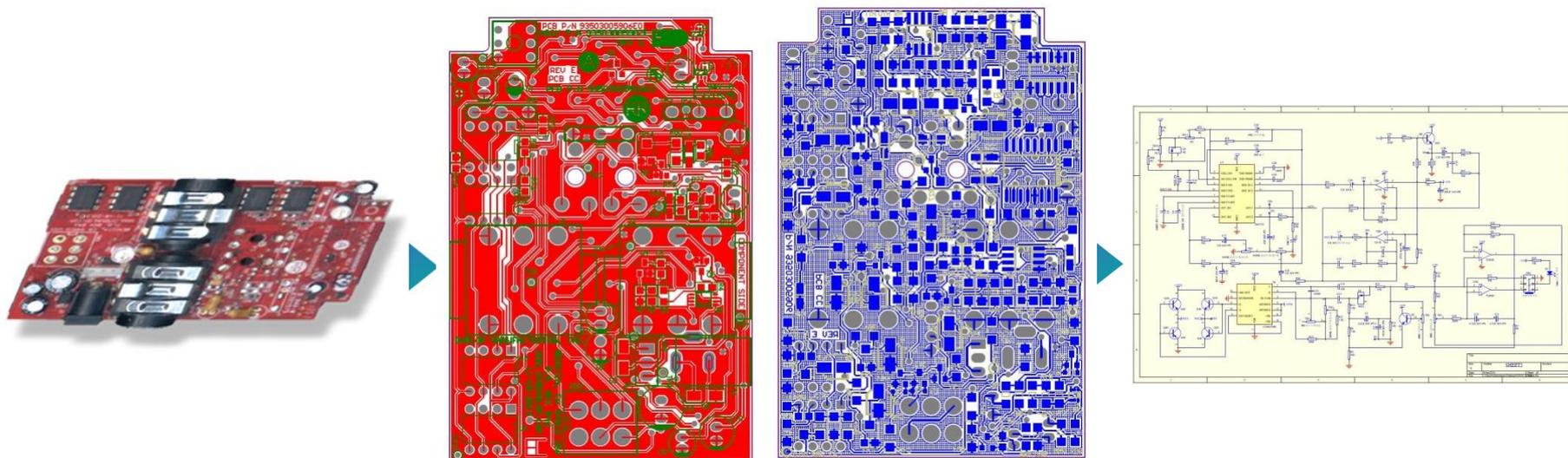


Layout trace from BGA



Layout trace from BGA

## ■PCB板分析 (PCB Analysis)



## 电路与版图设计相关专利

US07049860B2

**United States Patent**  
Gupta

(19) Patent No.: US 7,049,860 B2  
(45) Date of Patent: \*May 23, 2006

(54) METHOD AND CIRCUIT FOR CONTROLLING CURRENTS OF A FIELD EFFECT TRANSISTOR CONFIGURED TO CONDUCT A SIGNAL WITH VARYING VOLTAGE.

(72) Inventor: Sandeep K. Gupta, Mountain View, CA (US)

(73) Assignee: Broadcom Corporation, Irvine, CA (US)

(\*) Notice: Subject to any disclaimer, this patent is presumed to be available under 35 U.S.C. 102(b) by 10 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: 11/466,254  
(22) Filed: Feb. 28, 2005

(67) Prior Publication Data  
US 2005/0140973 A1 May 10, 2005

**Related U.S. Application Data**

(40) Continuation of application No. 10/752,978, filed on Feb. 23, 2004, now Pat. No. 6,561,833, which is a division of application No. 09/911,498, filed on Jul. 27, 2004, now Pat. No. 6,791,594.

(40) Divisional application No. 10/220,974, filed on Jul. 11, 2004.

(51) Int. Cl. G01F 27/02 (2006-01)

(52) U.S. Cl. 327/92; 327/337

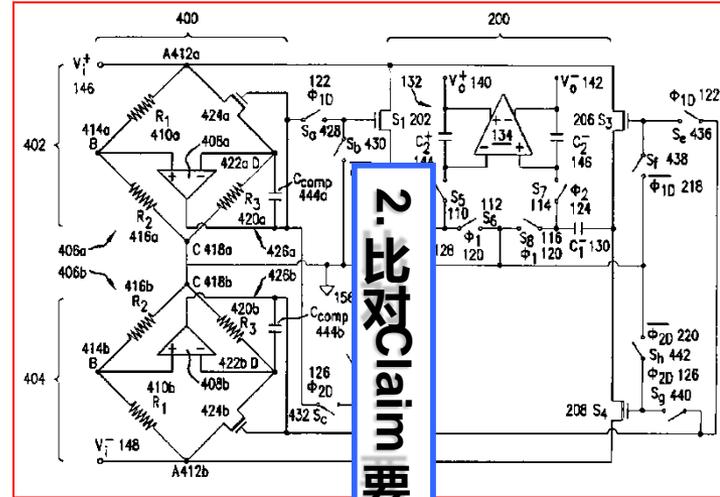
(58) Field of Classification Search: 327/337; 327/414; 328/430; 324/337; 310/343; 327/337; 2/3/12; 162/163; 209/201; 327/202; 225/504; 504/505; 505/191; 194/238  
See application file for complete search history.

**ABSTRACT**

The present invention relates to a replica network for linearizing switched source drivers. A bridge circuit with a MOSFET resistor is provided. A networking terminal of an operational amplifier is connected to a gate node of the bridge circuit and an inverting terminal of the operational amplifier is connected to a source node of the bridge circuit. The source nodes separated from the first node by another node of the bridge circuit. An output of the operational amplifier is provided to a gate terminal of the MOSFET resistor, and to the gate terminal of the MOSFET resistor in a switched capacitor circuit, thereby controlling the resistance of the MOSFET switch so that it is independent of the signal voltage. In this manner, the output network of the pre-driver is independent of the signal level. In this manner, the replica network of the present invention linearizes the switched source driver.

**2. 权利要求项**

**1. 找到相应专利**



## 制程相关专利

US07705776B2

**(12) United States Patent**  
Huang et al.

(10) Patent No.: **US 7,037,776 B2**  
(45) Date of Patent: **May 2, 2006**

(52) **SINGLE POLYSILICON PROCESS FOR DRAM**

(72) Inventors: **Jean-Ming Huang, Jinn-Chiu (J.W.) Chen, Aeng-Lin Hsiao (J.W.)**

(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu (TW)**

(71) Notice: Subject to any disclaimer, the title of this patent is considered to be amended under 35 U.S.C. 101(b)(2)(B).

(21) Appl. No.: **10/221,989**

(22) Filed: **Dec. 19, 2002**

(65) **Prior Publication Data**  
US 2004/011543 A1 11/17/04

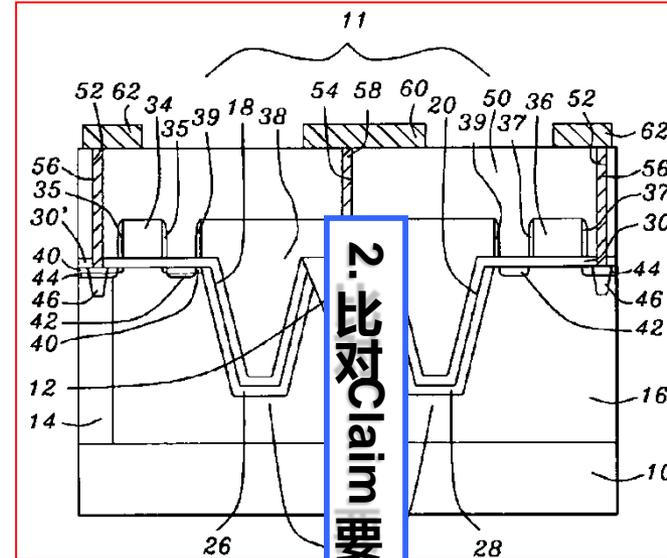
(51) Int. Cl. **H01L 21/8242 (2006.01)**

(52) **U.S. Cl. 438/243, 438/246, 438/248**

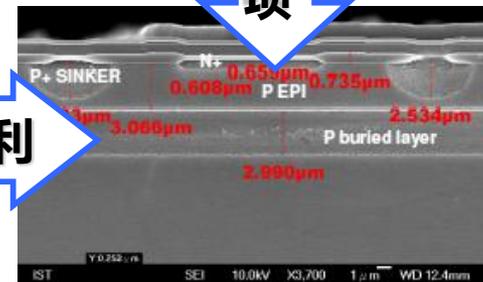
(58) **Field of Classification Search** 438/236, 379, 438/581, 377  
See also section 516 for complete search history.

(56) **References Cited**  
U.S. PATENT DOCUMENTS  
4,577,397 A 1/1990 Shih et al. 438/303

**45 Claims, 4 Drawing Sheets**



**1. 找到相应专利**



## 封装相关专利

112) **United States Patent**  
Yeh et al.

(10) Patent No.: **US 6,489,682 B1**  
(41) Date of Patent: **Dec. 3, 2002**

US 6,489,682 B1

(54) **BALL GRID ARRAY SEMICONDUCTOR PACKAGE AND SUBSTRATE THEREFOR**

(57) **Abstract**  
A BGA semiconductor package comprises a chip mounted on the central region of the upper surface of the substrate. The substrate includes an upper surface, a lower surface, a ground plate disposed on the upper surface, and at least one power plane disposed between the ground plate and the lower surface. A ground ring surrounds the periphery of the chip and possesses a first set of serrated rings extending toward the outer edge of the substrate. A first power ring surrounds the ground ring and possesses a second set of serrated rings extending among the first set of serrated rings of the ground ring, such that the extending portions of the first and second sets of serrated rings interlock essentially with each other and the wire bonding distances from the bonding posts on the upper surface to the extending portions of the first and the second serrated rings are comparable. According to another aspect of the present invention, a plurality of power vias are disposed and distributed in the power ring to electrically connect the power ring to the power plane, wherein at least two power vias are coupled together. The coupled power vias can reduce the damage to the weakness of ground plate this enables the best electrical performance of the ground plate.

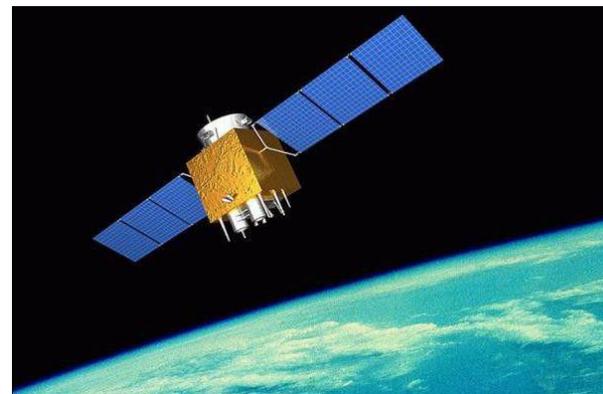
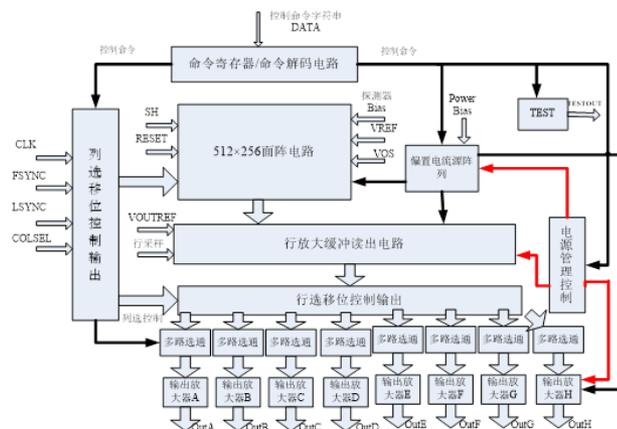
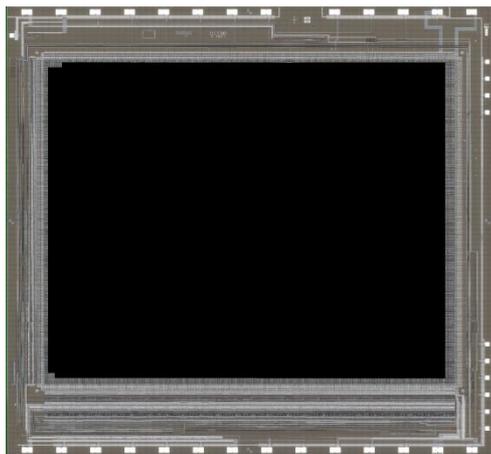
(73) **Assignee:** Advanced Semiconductor Engineering, Inc., Kaohsiung (TW)

(75) **Inventors:** Jung I. Yeh, Kaohsiung (TW), Shiu-Miao Jung, Kaohsiung (TW), Shian-Jaw Hsueh, Kaohsiung (TW)

(21) **Appl. No.:** 09/071,429  
(22) **Filed:** Sep. 27, 2000  
(51) **Int. Cl.:** H01L 23/40  
(52) **U.S. Cl.:** 257/338; 257/358; 257/374; 257/382  
(58) **Field of Search:** 257/337; 257/374; 257/382; 257/384; 257/386; 257/397; 257/398; 257/399; 257/400; 257/401; 257/402; 257/403; 257/404; 257/405; 257/406; 257/407; 257/408; 257/409; 257/410; 257/411; 257/412; 257/413; 257/414; 257/415; 257/416; 257/417; 257/418; 257/419; 257/420; 257/421; 257/422; 257/423; 257/424; 257/425; 257/426; 257/427; 257/428; 257/429; 257/430; 257/431; 257/432; 257/433; 257/434; 257/435; 257/436; 257/437; 257/438; 257/439; 257/440; 257/441; 257/442; 257/443; 257/444; 257/445; 257/446; 257/447; 257/448; 257/449; 257/450; 257/451; 257/452; 257/453; 257/454; 257/455; 257/456; 257/457; 257/458; 257/459; 257/460; 257/461; 257/462; 257/463; 257/464; 257/465; 257/466; 257/467; 257/468; 257/469; 257/470; 257/471; 257/472; 257/473; 257/474; 257/475; 257/476; 257/477; 257/478; 257/479; 257/480; 257/481; 257/482; 257/483; 257/484; 257/485; 257/486; 257/487; 257/488; 257/489; 257/490; 257/491; 257/492; 257/493; 257/494; 257/495; 257/496; 257/497; 257/498; 257/499; 257/500; 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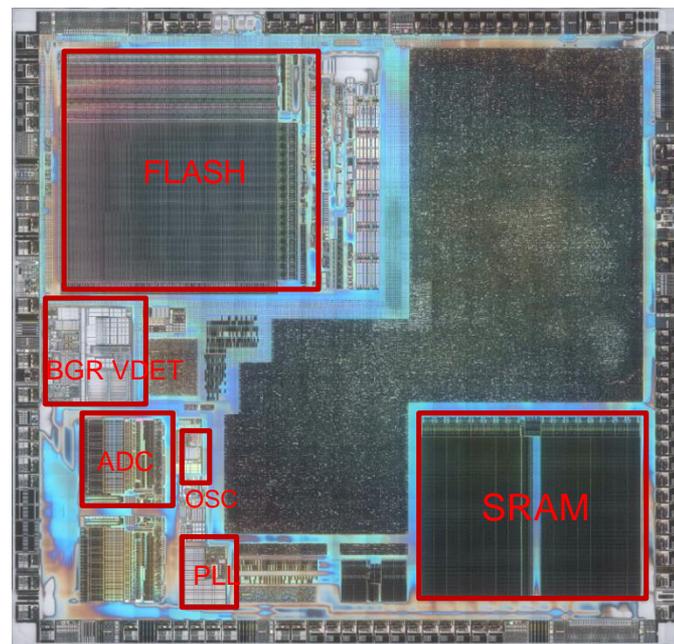
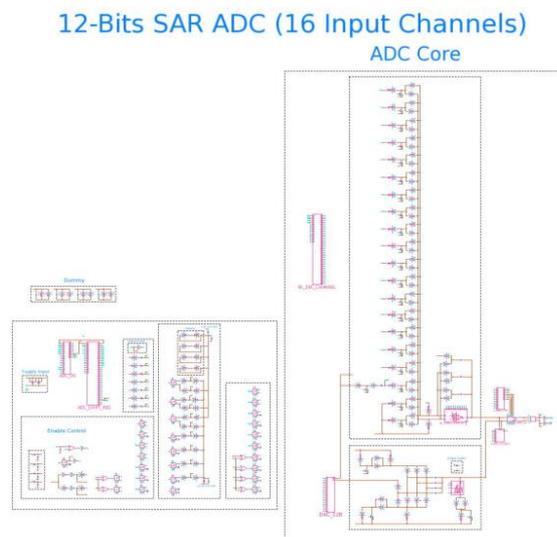
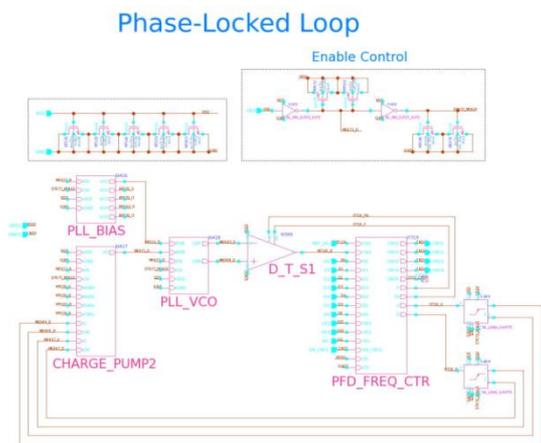
## 1: CMOS Image Sensor系列芯片

从2012年开始，对美国Indigo公司的320x256，640x512，1Kx1K等一系列不同规格、不同工作模式的红外图像传感器芯片进行了提取分析。2018年，客户在电路分析基础上，完全自主研发的某规格红外传感器芯片做为国家高分卫星上的核心芯片成功发射上天，成像性能超过指标要求，是军工航天类芯片通过竞品分析后消化吸收实现国产替代的典型案列。



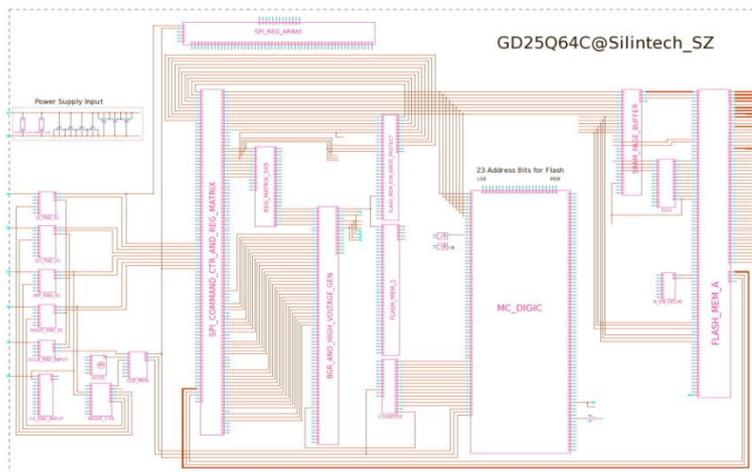
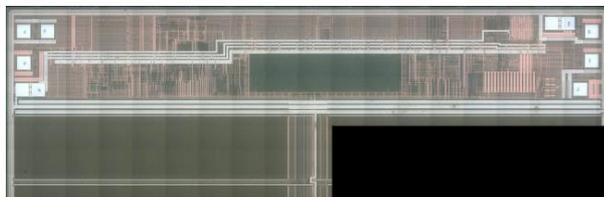
## 2: MCU系列芯片

2018年至今，解剖分析了意法半导体的STM32F103和STM32L476等多款基于ARM内核的32位MCU芯片，STM32系列是目前市场需要非常旺盛的系列芯片，迄今出货量有数十亿颗。对STM32F103做了除Memory以外的全芯片的电路提取，数字电路基于Cortex-M3内核，规模达到40万门。对模拟电路部分的架构和各模块实现做了整理与分析，主要模块包括I/O、POR、BGR、PVD、Digital Core VREG、HS OSC、LS OSC、PLL、Frequency Monitor、TPS、两个16通道输入的12-Bit SAR ADC模块等。



## 3: Flash存储芯片

2018年，解剖分析了一款具有SPI接口的64M Flash存储芯片，完成了全芯片的电路整理与分析。复原了芯片的顶层模块架构和底层模块的电路实现，包括5个高压电源和一个负压电源模块，及其过压和欠压保护，分析整理了SPI协议和指令寄存器的电路结构。完成了FLASH存储模块和SRAM Page Buffer存储模块的架构分析和读取译码电路的分析，配合数字电路的整理分析，定位了23位寻址总线、8位数据总线及其高低顺序，确定了读取实现原理。

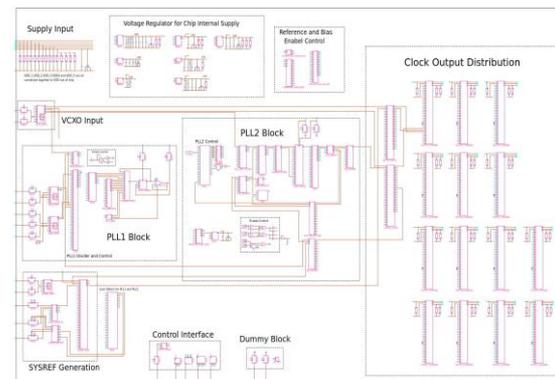
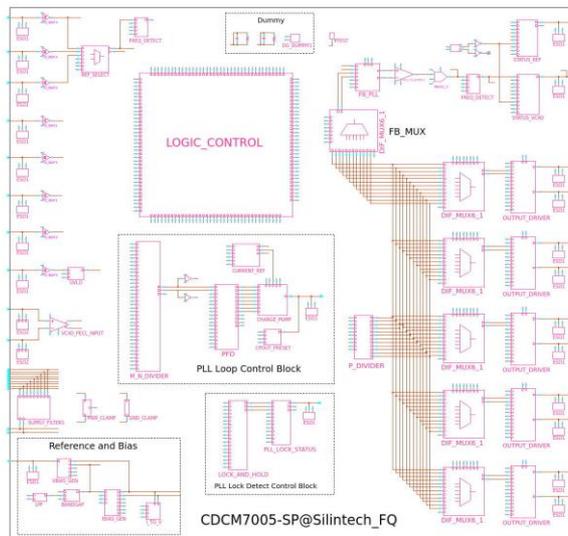
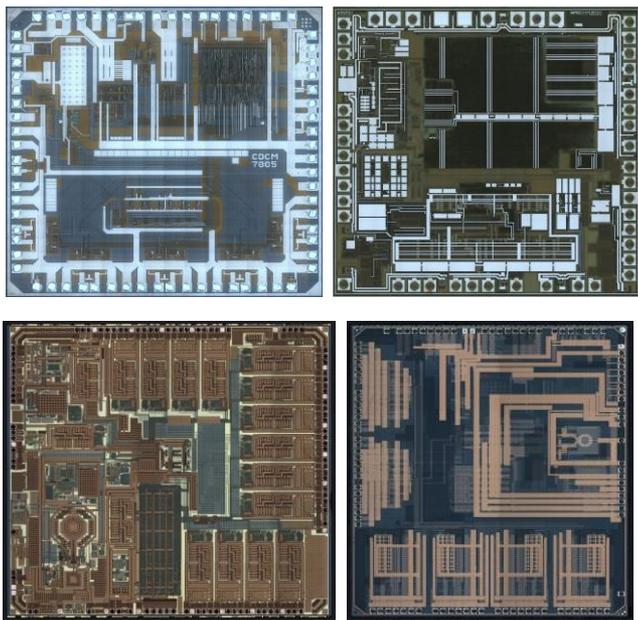


Flash Memory Array, Bit Line and Word Line Decode, and Read/Write Control



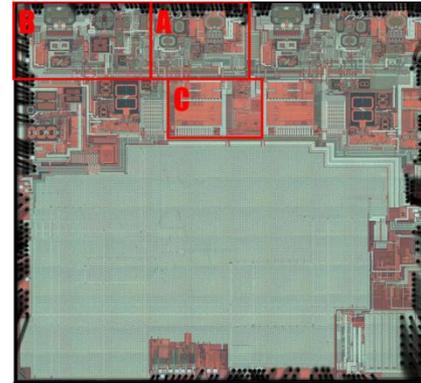
## 4: 高速锁相环系列芯片(PLL)

2017年至今，解剖分析了TI和ADI公司的一系列整数和小数锁相环芯片，包括了单级和两级锁相环架构，频率范围覆盖1GHz~8GHz。

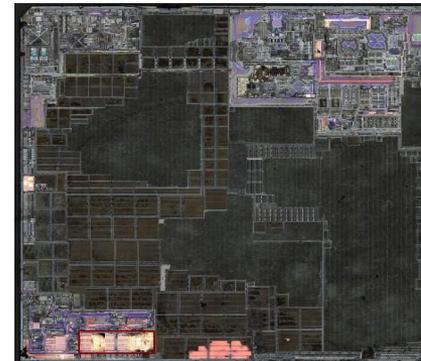


## 5: RF射频芯片

- Phase-Locked Loop (PLL) Synthesizers
- Wireless Transceiver
- RF Front-End Ics
- I/Q Modulators
- RF Mixer
- RF Switch
- RF Power Detector
- Variable Gain Amplifier
- Ethernet Transceiver



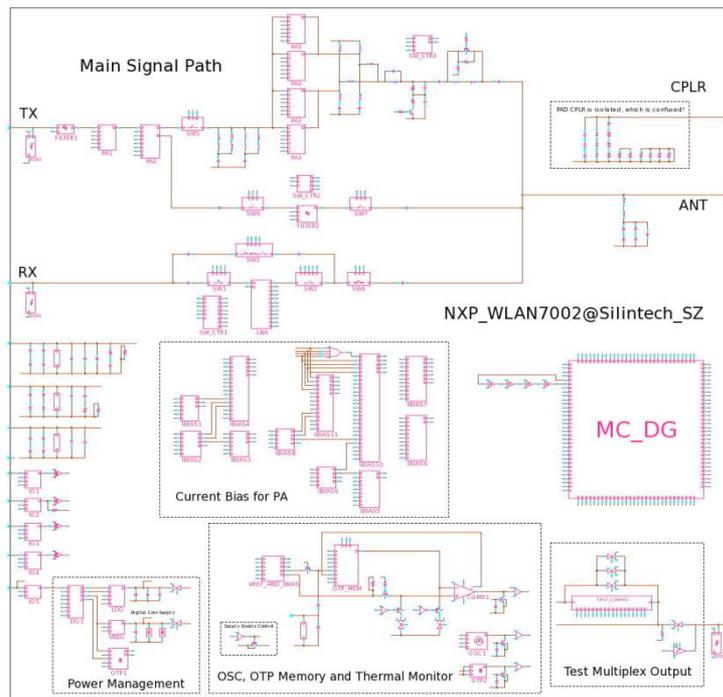
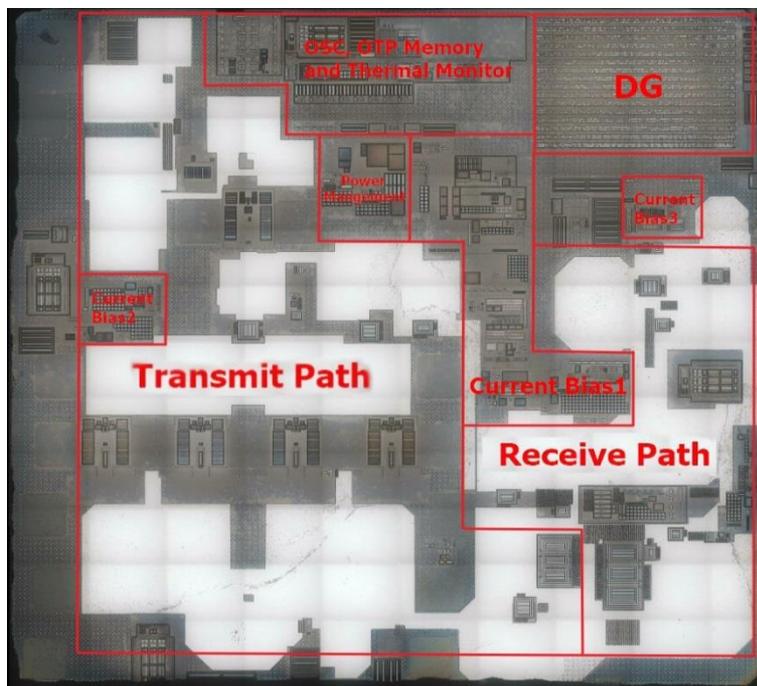
基于28nm工艺的  
MT7668



基于28nm工艺的  
Intel8260

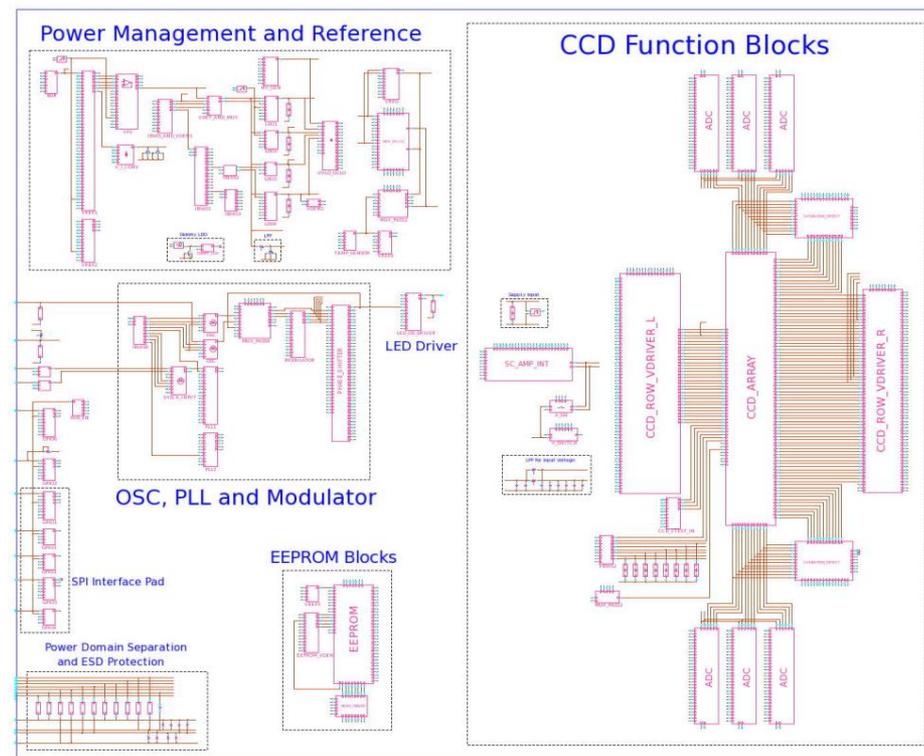
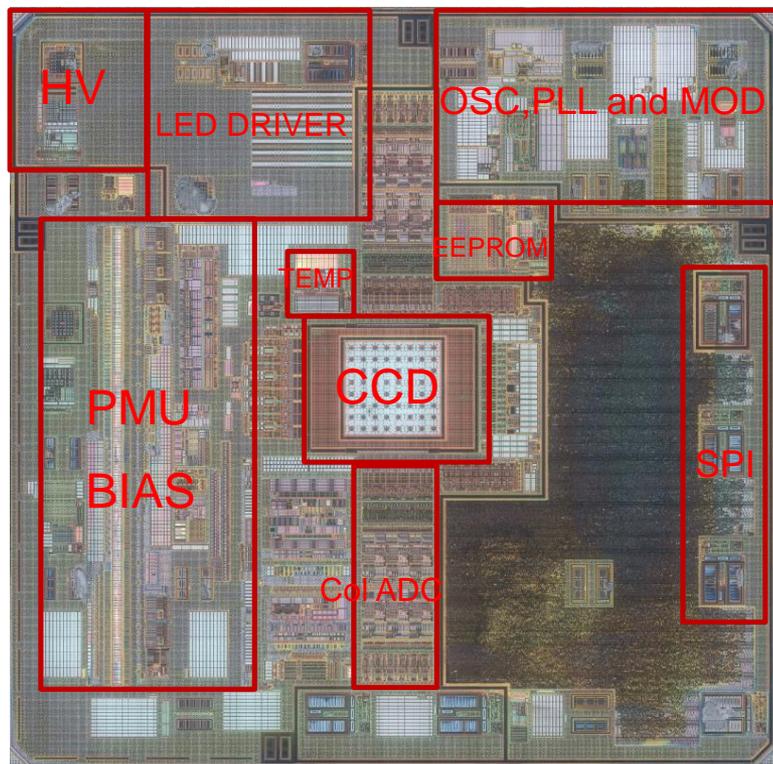
## 6、5G移动通讯应用的射频前端芯片(FEICs)

2019年完整的剖析了NXP公司最新的射频前端芯片WLAN7002，该芯片用于未来5G移动通讯应用，能支持IEEE 802.11 ax 高速协议。该芯片将功率放大器(PA)、低噪声放大器(LNA)、射频开关(Switch)、电源管理和控制电路集成在一颗die上，不再是多芯片模组封装，更高的集成度简化了系统设计，节省了移动设备中的空间占用。本芯片采用了0.18um SiGe BiCMOS工艺制造，电路上的级联设计和大量电源开关控制，提高了射频信号收发通道的柔性配置，并降低了芯片的整体功耗。



## 7: 3D深度传感器芯片(ToF)

2019年完成了瑞士Espros公司的epc611芯片的解剖分析，该芯片为目前市场上唯一一款光电集成在一体的飞行测距芯片(ToF)。ToF芯片未来将广泛应用于手机摄像、安防监控、工业视觉和无人驾驶等领域。



# THANK YOU



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